Testbench

module Traffic\_Light\_Controller\_TB;

reg clk,rst;

wire [2:0]light\_M1;

wire [2:0]light\_S;

wire [2:0]light\_MT;

wire [2:0]light\_M2;

Traffic\_Light\_Controller dut(.clk(clk) , .rst(rst) , .light\_M1(light\_M1) , .light\_S(light\_S)

,.light\_M2(light\_M2),.light\_MT(light\_MT) );

initial

begin

clk=1'b0;

forever #(1000000000/2) clk=~clk;

end

initial

begin

rst=0;

#1000000000;

rst=1;

#1000000000;

rst=0;

#(1000000000\*200);

$finish;

end

endmodule